ENHANCING DIGITAL AGE THROUGH TRI-GATE TRANSISTOR, FABRICATIONS AND APPLICATION

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Abstract
The 3D tri-gate transistors are a remarkable breakthrough in the realm of transistor technology. These transistors can be considered as reinvention of the transistor, because of the way they have supplanted the conventional "flat" 2D planar gate with an incredibly thin 3D silicon fin that rises up vertically from the silicon substrate. The tri-gate transistors have shown significantly improved electrostatics in terms of sub-threshold slope and drain induced barrier lowering and hence a better scalability than planar transistors. The Tri-gate transistors are the target of the next-generation technology, which target ultra-high-performance systems for military, wire line communications, cloud networking, and compute storage applications, as it enhances high level breakthrough in performance and power efficiency. These tri-gate transistors in contrast with other key semiconductor technologies will enable a new era of energy-efficiency. This Paper discusses the 3-D Tri-Gate transistor technology, its developments and integration with other silicon processing technologies, and its impact on the next generation high scale integrated circuit. Tri-Gate transistors are the first to be optimized into three-dimension and this marks a major revolution in the Semiconductor industry. The semiconductor industry continues to push technological innovation to keep pace with Moore's Law, shrinking transistors so that ever more can be packed on a chip. However, in future technology dispensation, the ability to shrink transistors will becomes more and more problematic, due to worsening short channel effects and an increase in parasitic leakages with scaling of the gate length dimension.

KEYWORDS:3-D transistor, 2-D planar, 22 NM Tri-gate.

Introduction

Transistors are microscopic, silicon-based switches that process the ones and zeros of the digital worlds and are the fundamental building block of all semiconductor chips. Tri-gate transistor is a MOSFET (metal-oxide-semiconductor field effect transistor) which incorporates three gates into a single device. It is a type of multiple gate field effect transistors (MUGFET). The three gates may be controlled by a single gate electrode, wherein the three gate surfaces act electrically as a single gate, or they can be operated independently.

For over 50 years, integrated circuits were using planar transistors as its core, during this period the size of the individual transistors has steadily decreased. Today, the transistor gate length in production is approximately 28 nanometres. But there are several limitations or drawbacks of these miniaturisations, most significant are: excessive gate leakage current, exponentially increasing source to drain sub-threshold leakage current, gate stack reliability and channel mobility

degradation from increasing electric field, rising dynamic power dissipation (CV2f) from non-scaled supply voltages, band to band tunnelling leakage at high body doping levels, device to device variation from random dopant fluctuation effects.

Compared to today's 65nm transistors, integrated tri-gate transistors can offer a 45 percent increase in drive current (switching speed) or 50 times reduction in off-current, and 35 percent reduction in transistor switching power.

In 2011 Intel Corporation announced production of new transistor technology called "3D Tri-Gate" that incorporated a three dimensional structure. The advancement resulted in faster on-off speeds and lower power without an increase in transistor size. At present, Intel Corporation is the only company to have made this design and manufacturing of transistors on 22 nm scale, and can provide data on the overall maturity and manufacturability of Tri-Gate transistors on a mass production scale. In February 2013, ALTERA and Intel Corporation jointly announced that the next generation of ALTERA's highest performance FPGA products would be manufactured using Intel's 14nm 3-D Tri-Gate transistor technology exclusively. Next generation FPGAs based on 14 nm Tri-Gate design will enjoy benefits from both, the transistor geometry shrink, 14nm and density improvements as allowed by 3-D Tri-Gate transistor design.

DESCRIPTION OF TRI-GATE TRANSISTORS

Tri-gate is the terms used by Intel Corporation to describe their non-planar transistor architecture planned for use in future microprocessors. These transistors employ a single gate stacked on top of two vertical gates allowing three times the surface area for electrons to travel. Intel reports that their tri-gate transistors reduce leakage and consume far less power than current transistors. This allows up to 37% higher speed, and low power consumption.

The additional control enables as much transistor current flowing as possible when the transistor is in the 'on' state and as close to zero as possible when it is in the 'off state (to minimize power), and enables the transistor to switch very quickly between the two states. it utilizes multiple fins to increase the drive strength for increased performance.

Figure 1.a shows the design with just a single fin while that of figure 1.b and figure 1.c shows the design of two and three fin.

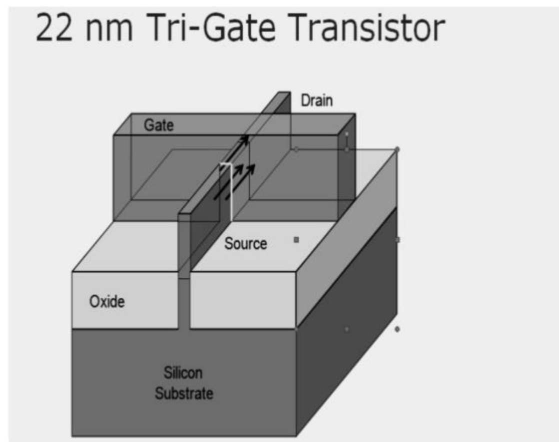


Figure 1.a Design with a Single Fin

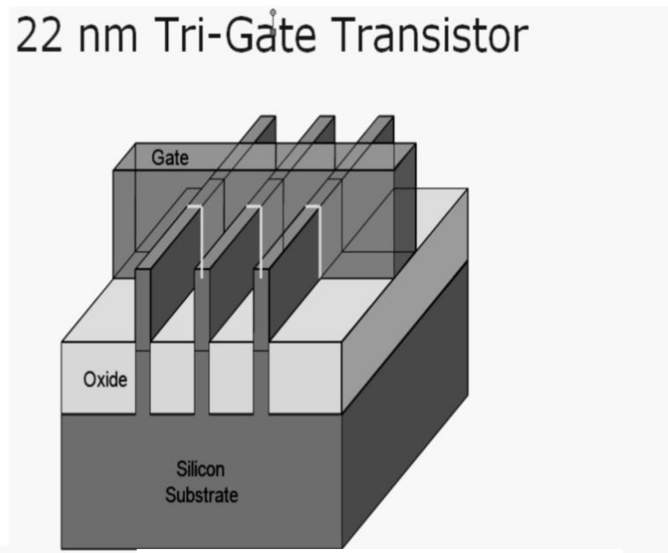


Figure 1.b Design with a Three Fin

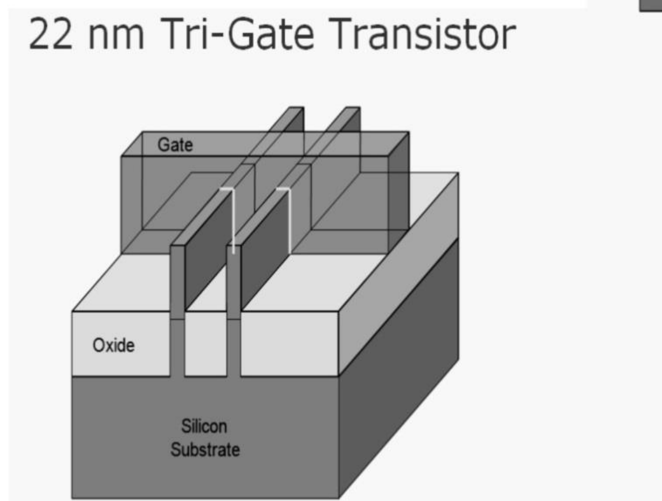
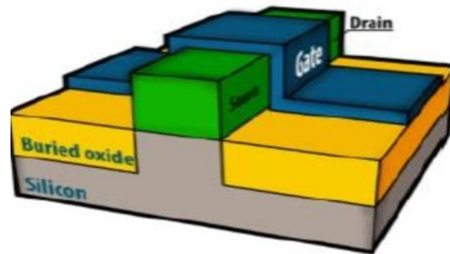


Figure 1.c Design with a Two Fin

dimension of cell is further minimized and additional scaling of transistor is being done for better packaging on a given chip. In order to improve the short channel resistance and stability, a tri-gate transistor is required. The configuration of tri-gate transistor is designed in a way that they are fully depleted even before reaching the threshold point; the complete Silicon present under the gate electrode is depleted of carriers. Tri-gate transistors have expressively developed electrostatics in terms of sub-threshold slope, drain induced barrier lowering and better scalability as compared to planar single gate transistors.



The structure of Tri-gate transistor represents a fundamental departure from the 2D planar transistor structure as shown in Fig.2. Tri-gate transistors form conducting channels on three sides of a vertical fin structure, thus they are fully depleted so that the entire available silicon underneath the gate electrode is depleted of carriers before the threshold condition is reached.

Since fins are made vertical in nature, high packing density can be achieved, by packing transistors closer together. Further, to get even more performance and energy-efficiency gains, designers also have the ability to continue growing the height of the fins.

Tri gate transistor can be fabricated either on the SOI substrate or standard bulk-silicon substrate. It has one gate electrode on the top and other two gate electrodes on the sides of the silicon body. This additional gate control enables as much transistor current flowing as possible when the transistor is in the 'on' state and as close to zero as possible when it is in the 'off state and enables the transistor to switch very quickly between the two states.

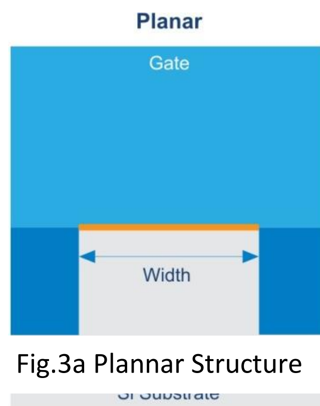


Fig.3a Plannar Structure

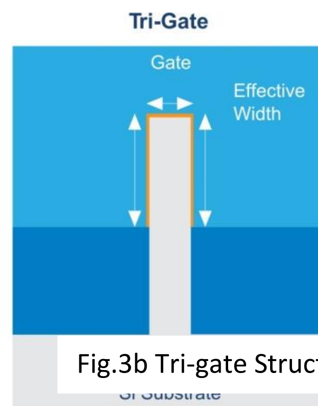


Fig.3b Tri-gate Structure

The key performance advantage of Tri-Gate transistor geometries over traditional planar geometries can be found in the effective width of the conducting channel.

Figure 3a shows a cross-sectional representation of a traditional transistor. Its gate is built in a single plane (thus the name "planar"). The effective width of the channel is shown in yellow. Fig.3b shows a 3D tri-gate transistor, demonstrating how a greater channel width is achieved from the 3-D structure without increasing the overall footprint of the transistor, which results in higher performance without increased the area.

Without any impact on the layout area, designers have a choice of extending the width in third dimension in tri gate transistor

structure; as a result the effective channel width can be significantly enhanced relative to a planar transistor.

Effective channel length and the effective fin width of the device are used as the key knob for controlling the short channel effects in 3D transistors. Device designers design electro-statically well controlled 3D transistors by keeping the effective channel length to fin width ratio greater than 0.5. This also allows them to reduce the channel doping which, in turn, reduces the impurity scattering the channel, enhances volume inversion effect and results in higher performance, particularly at lower bias region.

Besides these advantages, there are several known issues and characteristics of the 3-D gate structure, which include the modelling of new parasitic capacitance values not modelled in traditional planar designs, layout dependent effects, and the use of double-patterning techniques.

Integration of TRI-Gate design with other Technologies

For improving the efficiency, the tri-gate design is enhanced by using both high-k gate insulators with metal gates to improve both ON and OFF currents, and adding strained silicon for enhanced mobility also improving device performance.

Non-planar transistor integrated with other silicon process technologies can provide 30 percent higher NMOS drive current and 60 percent higher PMOS drive current than the optimized, state-of-the-art 65nm-node planar transistors at the same off-state leakage.

NMOS receives benefit from tensile strain.

High-k/Metal-gate Technology

The term high-k dielectric refers to a material lwith a high dielectric constant as compared to silicondioxide. The tri-gate CMOS transistors use a high-k material to replace the transistor's traditional silicondioxide dielectric, and also replace the conventional poly-silicon gate electrode with metal gate electrodes with work function close to the mid gap. Replacing the silicon dioxide gate dielectric with a high-K material lallows increased gate capacitance without the associated leakage effects.

The metal gate technology eliminates poly-silicon depletion and enhances transistor performance. In addition, the use of metal electrodes with close-to-mid gap work functions also allows the reduction of substrate doping concentrations, thus enhancing transistor overall transistor performance.

Dual epitaxial raised source/drain structure

Through epitaxial deposition, the integrated CMOS tri-gate transistor creates a unique source/drain structure, in which epitaxial deposition of silicon is done for NMOS transistor and Si-Ge for PMOS transistor.

For reducing the parasitic resistance, the source and drain regions are raised with respect to the plane of the gate oxide-silicon substrate interface. This improves device performance. Intel has manufactured prototypes of the integrated tri-gate CMOS transistors on SOI as well as bulk-silicon substrates. The tri-gate transistor on bulk silicon and on SOI demonstrates equivalent scaling and short-channel performance and transistor drive performance.

Fig. 4 shows that 22nm 3D tri-gate transistor will be 37% faster at low voltages than 32nm planar transistor. These transistors can operate at lower voltages, hence saving more than 50%of power compared to 32nm planar transistor. This makes them ideal for use in small handheld devices, which operate using less energy to "switch" back and forth.

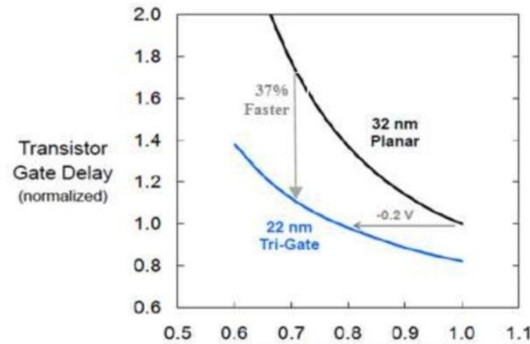


Fig.4 Graph of Transistor Gate Delay vs. Operating Voltage.

Fig. 5 illustrates the channel current in a Tri-Gate transistor vs. a planar transistor as a function of gate voltage. When the gate voltage is at 0 V, there is an order of magnitude lower amount of leakage current flowing through the channel of the Tri-Gate transistor compared to the planar transistor. Thus the Tri-Gate transistor effectively minimises the leakage power.

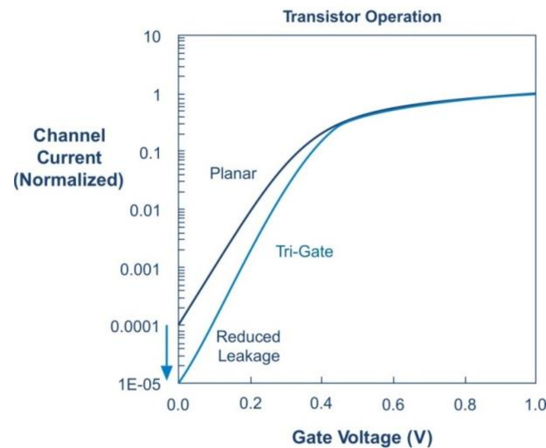


Fig. 5 Graph of channel current vs gate

Due to lower supply voltage requirement, control over the static and active power dissipation of in tri-gate transistors this improves tremendously the efficiency of devices utilizing tri-gate. Figure 6 shows this active power reduction; the trend in active power across process nodes has been in the downward direction. However, as demonstrated by the bend in the curve further downward from the 32 nm planar node, the introduction of Tri-Gate transistors has clearly further reduced the dynamic power beyond the trend established by prior process geometry shrinks.

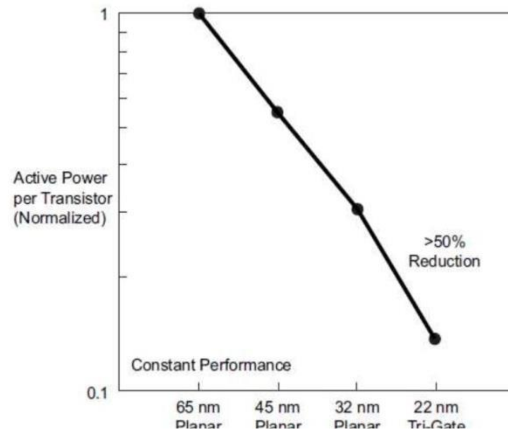


Fig.6 Graph of Active Power in Planar and Tri-Gate Transistors.

Other benefits of 3D tri-gate technology includes: Improved defect density curves in 22nm Tri-Gate as compared to 32 nm planar design and reductions in SEU incidence rates from four times to ten times when moving from 32 nm planar to 22 nm Tri-Gate design.

Improving Performance with Integrated Tri-Gate Transistors

In benchmark testing, Intel demonstrated that integrated tri-gate NMOS and PMOS transistors showed excellent control of short channel effects (SCE), leading to reduced parasitic leakages and decreased power consumption. The tri-gate transistors also demonstrated higher performance, in terms of drive current, compared to an optimized, state-of-the-art planar 65nm-node transistor. For a given transistor off-state leakage current (Iqff), the integrated tri-gate NMOS transistor had 30 percent higher drive current (Idsat) than the planar transistor. This effect is even more pronounced for the integrated tri-gate PMOS transistor, which produced 60 percent higher drive current than the planar transistor at a given Iqff
(Ferain, 2011)

Literature Review

In 1947 the first transistor, a germanium 'point-contact' structure, was demonstrated at Bell Laboratories. Silicon was first used to produce bipolar transistors in 1954, but it was not until 1960 that the first silicon metal oxide semiconductor field-effect transistor (MOSFET) was built. The earliest MOSFETs were 2D planar devices with current flowing along the surface of the silicon under the gate. The basic structure of MOSFET devices has remained substantially unchanged for over 50 years. (Lime, 2003)
Since the proclamation of Moore's Law in 1965, many additional enhancements and improvements have been made to the manufacture and optimization of MOSFET technology in order to enshrine Moore's Law in the vocabulary and product planning cycles of the semiconductor industry. In the last 10 years, the continued improvement in MOSFET performance and power has been achieved by breakthroughs in strained silicon, and High-K metal gate technology. The potential for 3-D, or 'wraparound' gate transistor technology, to enhance MOSFET performance and eliminate short channel

effects, was recognized. This paper called the proposed 3-D structure 'depleted lean-channel transistor', or DELTA In 1997 the Defense Advanced Research Projects Agency (DARPA) awarded a contract to a research group at the University of California, Berkeley, to develop a deep sub-micro transistor based on the DELTA concept. One of the earliest publications resulting from this research in 1999 dubbed the device a 'FinFET' for the fin-like structure at the center of the transistor geometry. (Suman, 2013)

The main Advantages of tri-gate transistor

- Lower leakage and consume much less power.
- 45% increase in on/off speed.
- The basic building blocks of future microprocessors.
- Moore's law scaling can be taken well into next decade.
- They offer considerably lower leakage and consume much less power than today's planar transistors.
- Faster & cooler operation.
- 50% reduction in off-current
- 35% reduction in total power at constant speed
- Tri-gate gives better off current and therefore less wasted power
- High k metal gate gives both higher speed and less wasted power
- Strained Si produces higher speed and less wasted power
- Tri-gate Shows Improved Scalability.

Application on tri-gate transistor

- Critical part of Intel's Energy efficient performance.
- Scaling of silicon transistors.
- Increase battery life of mobile devices.

Summary

As transistors get smaller, parasitic leakage currents and power dissipation become significant issues. By integrating the novel three-dimensional design of the tri-gate transistor with advanced semiconductor technology such as strain engineering and high-k/metal gate stack, Intel has developed an innovative approach toward addressing the current leakage problem while continuing to improve device performance. The integrated CMOS tri-gate transistors will play a critical role in Intel's energy-efficient performance philosophy because they have a lower leakage current and consume less power than planar transistors. Because tri-gate transistors greatly improve performance and energy efficiency, they enable Intel to extend the scaling of silicon transistors. Intel expects that the tri-gate

Conclusion

3D Tri-Gate technology by Intel is an important innovation needed to continue Moore's Law. The Tri- gate technology if embrace with semiconductor technologies like; strain engineering, high k/metal gate it will yield high performance semiconductor device product. Dual epitaxial raised source/drain structure etc. delivers unprecedented performance improvement and power reduction in semiconductor devices. However, no single process technology can meet all the diverse requirements needed. Though 3D Tri-Gate technology will be a foundation of next generation of semiconductor devices to provide the highest core performance at the lowest power, it may not be the optimal solution for everyone. There are other technologies such as TSMC's 20SoC and 55 EmbFlash that can complement Intel's Tri-Gate technology.

Identifying the highest performance semiconductor devices products has

historically been a subjective and parametric benchmarking process. But beginning with 14 nm Tri-Gate technology, the highest performance semiconductor devices will simply be the ones built on demonstrably superior transistor technology. Only Intel's 14 nm Tri-Gate Process offers a second generation of proven production technology. Only Intel's 14 nm processesprovide both the benefit of the Tri-Gate technology as well as the benefits of a full transistor process shrink. And, Intel is the only major semiconductor company with access to this technology. Designing systems using Tri-Gate based technology will ensure that designers can take advantage of this performance leadership.

RECOMMENDATION

For higher institution students to improve their selves on 3-D transistor to get smaller, parasitic leakage currents and power dissipation become significant issues. By integrating the novel three-dimensional design of the tri-gate transistor with advanced semiconductor technology such as strain engineering and high-k/metal gate stack, Intel has developed an innovative approach toward addressing the current leakage problem while continuing to improve device performance. Because tri-gate transistors greatly improve performance and energy efficiency, they enable to extend the scaling of silicon transistors. For federal government of Nigeria to Intel expects that the tri-gate transistors could become the basic building block for microprocessors in future technology nodes. The technology can be integrated into an economical, high-volume manufacturing process, leading to high-performance and low-power products.

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